IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Darmawan

Application No.: 10/053,424

Filed: November 2, 2001

Title: SILICON ON INSULATOR DEVICE WITH IMPROVED HEAT REMOVAL (As amended)

Attorney Docket No.: CREEP027/P02111

Examiner: Tran, Tan N.

Group: 2826

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on January 13, 2004 in an envelope addressed to the Commissioner for Patents, Mail Stop Appeal Brief-Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: Kristina Gomez

Kristina Gomez

APPEAL BRIEF TRANSMITTAL
(37 CFR 192)

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This brief is in furtherance of the Notice of Appeal filed in this case on January 13, 2004. This brief is transmitted in triplicate.

This application is on behalf of

☐ Small Entity ☒ Large Entity

Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

☐ $165.00 (Small Entity) ☒ $330.00 (Large Entity)

☐ Applicant(s) hereby petition for a _____ extension(s) of time to under 37 CFR 1.136.

If an additional extension of time is required, please consider this a petition therefor.

☐ An extension for months has already been secured and the fee paid therefor of $ is deducted from the total fee due for the total months of extension now requested.

☒ Applicant(s) believe that no (additional) Extension of Time is required; however, if it is determined that such an extension is required, Applicant(s) hereby petition that such an

extension be granted and authorize the Commissioner to charge the required fees for an Extension of Time under 37 CFR 1.136 to Deposit Account No. 500388.

Total Fee Due:	
Appeal Brief fee	$330.00
Extension Fee (if any)	$
Total Fee Due	$330.00

☒ Enclosed is Check No. 21199 in the amount of $330.00.

☒ Charge any additional fees or credit any overpayment to Deposit Account No. 500388, (Order No. CREEP027). Two copies of this transmittal are enclosed.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Henry K. Woodward
Reg. No. 22,672

P.O. Box 778
Berkeley, CA 94704-0778
(650) 961-8300

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE DARMAWAN

Application for Patent

Filed November 2, 2001

Serial No. 10/053,424

FOR:

SILICON ON INSULATOR DEVICE WITH IMPROVED HEAT REMOVAL (AS AMENDED)

APPEAL BRIEF

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on January 13, 2004 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signed: Kristina Gomez

BEYER WEAVER & THOMAS, LLP
Attorneys for Applicant

01/20/2004 HDEMESS1 00000061 10053424
02 FC:1402 330.00 OP

TABLE OF CONTENTS

Page No.

This is an appeal from the Office Action mailed October 27, 2003, finally rejecting claims 15 and 21-23 in the above-identified patent application. A copy of the claims on appeal are in the attached appendix.

I. REAL PARTY IN INTEREST

The real party in interest is Cree Microwave, Inc., by change of name from Ultra RF, Inc., of Sunnyvale, CA, assigned from Johan August Darmawan, inventor and applicant.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences

III. STATUS OF THE CLAIMS

Method claims 1-14 are being prosecuted in divisional patent application serial no. 10/327,479, device claims 16-20 are cancelled and claims 15 and 21-23 as amended remain in the application.

IV. STATUS OF AMENDMENTS

No amendment has been filed subsequent to this second final rejection.

V. SUMMARY OF INVENTION

The invention relates generally to silicon on insulator (SOI) semiconductor devices and manufacturing processing. As described in the background of the invention, reduced parasitic components can be achieved in semiconductor devices by fabrication of the devices in a silicon on insulator structure, such as silicon on sapphire and silicon on oxide insulator , including commercially available bonded silicon on insulator and implanted oxide (SIMOS). In such structures the supporting substrate is typically bonded to a heat sink for heat removal, which is particularly important for power transistor structures. Additionally, a ground plane can be provided by metallization on the substrate surface.

The claimed invention is directed to an SOI device having improved heat removal and with a structure which facilitates manufacture. With reference to Fig. 1D (copy as

exhibit 2 in the appendix) in one embodiment a component such as a transistor 16 is fabricated in silicon layer 14 which is supported by substrate 10 with a silicon oxide layer 12 therebetween. A heat sink for component 15 comprises a metal layer including refractory metal 20 and a metal layer 22. Metal layer 22 can be gold, copper, or aluminum, for example, which is compatible in semiconductor device and integrated circuit structures and manufacturing processes. The refractory metal 20 is optional in the structures.

An important feature of the invention is the provision of metal 20, 22 in a recessed portion of substrate 10 in close proximity to component 16 and insulated therefrom by silicon oxide layer 12. Further, as shown in Fig. 1c, the recessed portion in substrate 10 is formed by a preferential etchant which etches substrate 10 and with silicon oxide layer 12 functioning as an etchant stop, thereby preventing over etching into silicon oxide layer 12 and silicon layer 14.

Thus, in accordance with the invention as defined by claim 15, a metal layer is formed in the portion of the substrate in which silicon has been removed by etching, the metal layer abutting the silicon oxide layer and providing heat removal from the component, the silicon oxide layer electrically insulating the metal layer from the semiconductor component. Claims 21-23 further define the metal layer.

VI. ISSUES

Claim 15 has been finally rejected under 35 USC 102(e) as fully met and anticipated by Udrea et al., U.S. Patent Application Publication No. US 2002-0041003, the Examiner referring to Figs. 10a and 13c and the electrically insulating heat sink 45 in both figures.

Claims 21-23 have been finally rejected under 35 USC 103(a) as being unpatentable over Udrea et al. in view of Lin, U.S. Patent No. 6,483,147, the Examiner referring to Figs. 10a and 13c and paragraph **[0040]** of Udrea et al. and metal layer 52 in Lin.

The two issues in this appeal are whether Udrea et al. disclose the invention as defined by independent claim 15 and whether Udrea et al. can be modified by the teachings of Lin to suggest the invention as defined by dependent claims 21-23.

VII. GROUPING OF CLAIMS

The claims in each group stand together.

VIII. ARGUMENT

THE SILICON ON INSULATOR (SOI) SEMICONDUCTOR DEVICE AS DEFINED BY CLAIM 15 IS NOT DISCLOSED OR SUGGESTED BY UDREA ET AL.

The basic distinction between the device as defined by claim 15 and the device defined by Udrea et al. as shown in Figs. 10a and 13c is straight forward.

Claim 15 recites:

> a) a semiconductor body including a silicon supporting substrate, a silicon oxide layer supported by the substrate, and a silicon layer overlying the silicon oxide layer,
>
> b) a semiconductor component formed in the silicon layer overlying a portion of the substrate in which silicon has been removed by etching, and
>
> c) a **metal layer** in the portion of the substrate in which silicon has been removed by etching, the metal layer abutting the silicon oxide layer and providing heat removal from the component, **the silicon oxide layer electrically insulating the metal layer from the semiconductor component.** (Emphasis added).

The recited metal layer for heat removal is compatible with semiconductor device fabrication and facilitates heat removal by being placed close to the semiconductor component but electrically insulated therefrom.

Udrea et al. discloses in Figs. 10a and 13a an active structure 18 of a power device 10 which also includes an insulating membrane 16, also labeled 50 in Figs. 10a and 13c, and a heat sink material 45 contacting membrane 50. However, Udrea et al. expressly describes the heat sink material 45 as an insulating layer. See paragraphs **[0076]** and **[0079]**. Indeed, Udrea et al. describe heat layer 45 as diamond, aluminum oxide, boron nitride, or other materials with good electrically insulating properties and high thermal conductivity. See paragraphs **[0039]**, **[0074]** and **[0118]**, which are cited by the Examiner. Such insulating materials are not a metal layer as recited in claim 15 and are apparently intended to be transparent to infrared wavelengths, as suggested in paragraph **[0017]**. Accordingly, it is respectfully submitted that Udrea et al. do not show or suggest the semiconductor device as defined by claim 15.

DEPENDENT CLAIMS 21-23 ARE NOT SUGGESTED BY UDREA ET AL. IN VIEW OF LIN

Claims 21-23 depend from claim 15 and further define the metal layer of claim 15 as comprising a refractory metal, such as titanium tungsten and further comprising gold, aluminum or copper over the refractory metal.

Lin describes a backside metal contact to a SOI semiconductor device in which the contact comprises a conductive plug 38 that electrically contacts the semiconductor device 32 through a hole in silicon substrate layer 12 and insulation layer 34. Thus the contact is intended to be an electrical terminal of the device and necessarily physically and electrically contacts the device.

This is not the structure or function of the metal layer in the claimed invention where a silicon oxide layer electrically insulates the metal layer from the semiconductor component. While the invention leaves the insulating layer intact and thereby functions as an etch stop in etching the substrate, Lin intentionally removes the insulation layer so that the conductive plug 38 electrically and physically contacts the semiconductor device 32. This feature is specifically claimed by Lin, in particular reciting, "a conductive plug through the silicon substrate layer and the insulation layer contacting the silicon device layer, wherein the conductive plug extends into the silicon device layer."

Udrea et al. do suggest that the heat sink could be a bottom terminal of the semiconductor device and would be electrically and thermally conductive. This is similar to the conductive plug 38 of Lin which functions as a bottom terminal of the semiconductor device. However, in the claimed invention, the metal layer functions only as a heat sink and is expressly electrically insulated from the semiconductor component.

Accordingly, it is respectfully submitted that the teachings of Lin cannot be combined with Udrea et al. to suggest the invention as defined by claims 21-23.

IX. CONCLUSION

The silicon on insulator semiconductor device as defined by claims 15 and 21-23 is neither shown nor suggested by Udrea et al. alone or taken with Lin. The rejections of claims 15 and claims 21-23 under 35 USC 102(e) on Udrea et al., and under 35 USC 103(a) on Udrea et al. in view of Lin, should be reversed.

Respectfully Submitted,
BEYER WEAVER & THOMAS, LLP

Henry K. Woodward
Registration No. 22,672

BEYER WEAVER & THOMAS, LLP
P.O. Box 778
Berkeley, CA 94704-0778
(650) 961-8300

X. APPENDIX

CLAIMS ON APPEAL

Claims 1-14 (Withdrawn).

15. A silicon on insulator (SOI) semiconductor device comprising:

a) a semiconductor body including a silicon supporting substrate, a silicon oxide layer supported by the substrate, and a silicon layer overlying the silicon oxide layer,

b) a semiconductor component formed in the silicon layer overlying a portion of the substrate in which silicon has been removed by etching, and

c) a metal layer in the portion of the substrate in which silicon has been removed by etching, the metal layer abutting the silicon oxide layer and providing heat removal from the component, the silicon oxide layer electrically insulating the metal layer from the semiconductor component.

Claims 16-20 (Cancelled).

21. The semiconductor device and defined by claim 15, wherein the metal layer comprises a refractory metal.

22. The semiconductor device as defined by claim 21, wherein the metal layer comprises gold, aluminum, or copper over the refractory metal.

23. The semiconductor device as defined by claim 21, wherein the refractory metal comprises titanium tungsten.

FORMAL DRAWINGS

Formal Drawings are attached hereto.

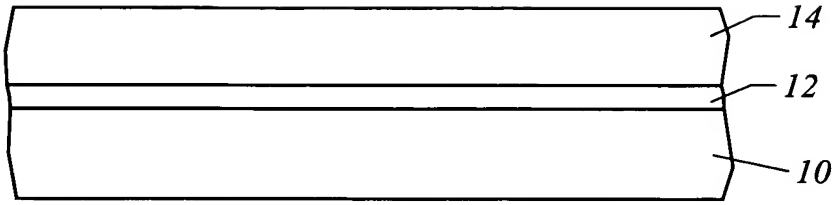

FIG. 1A

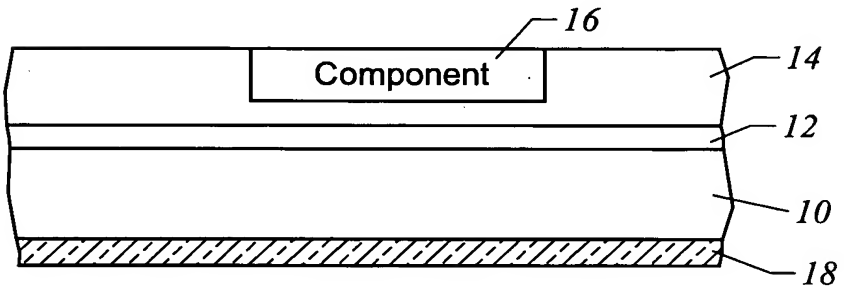

FIG. 1B

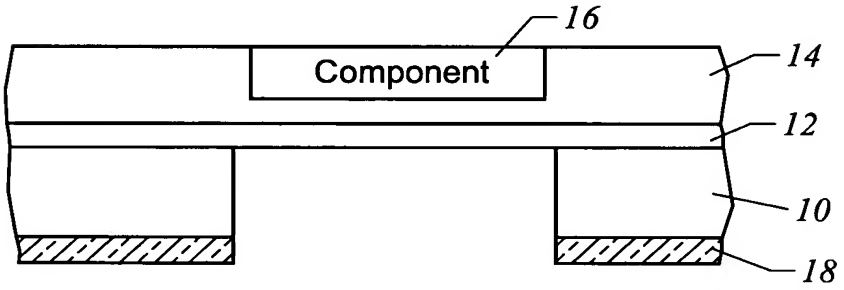

FIG. 1C

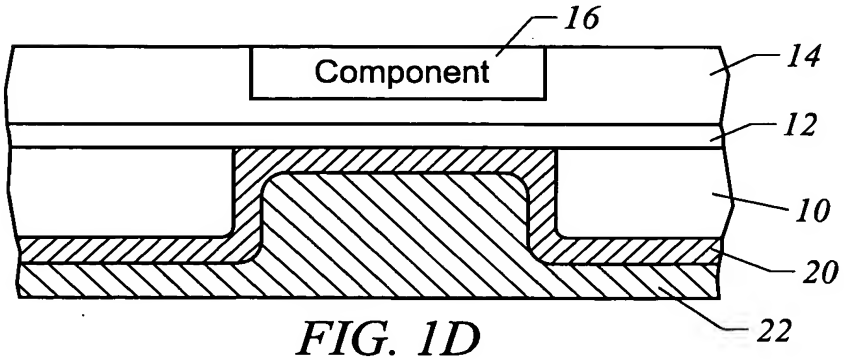

FIG. 1D

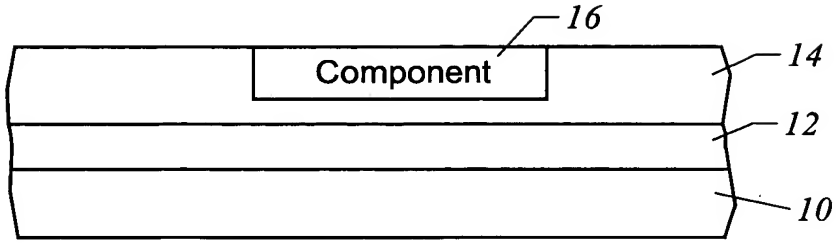

FIG. 2A

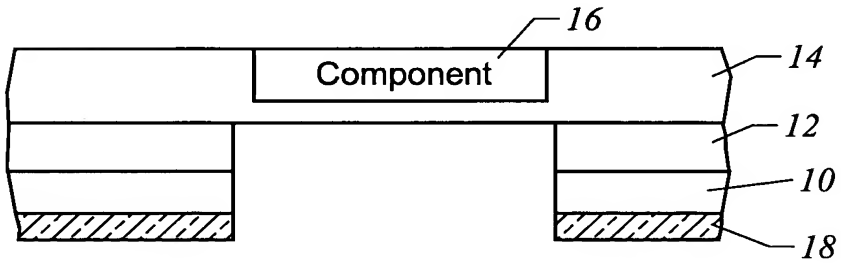

FIG. 2B

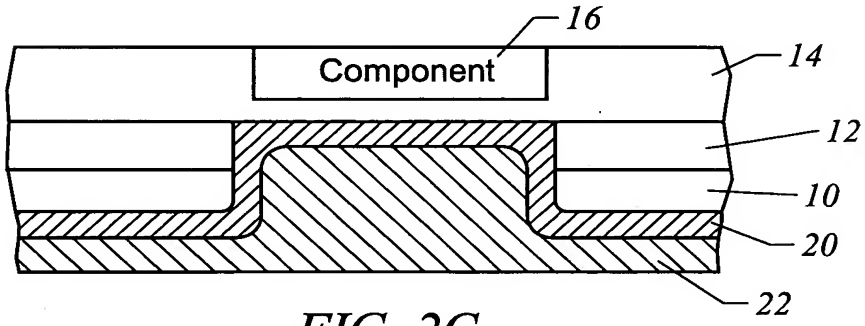

FIG. 2C

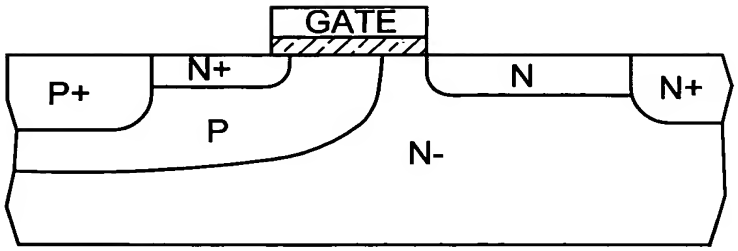

FIG. 3A

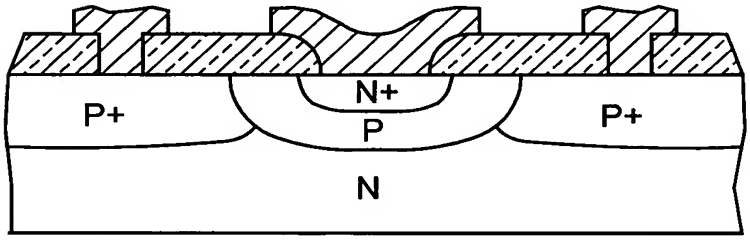

FIG. 3B

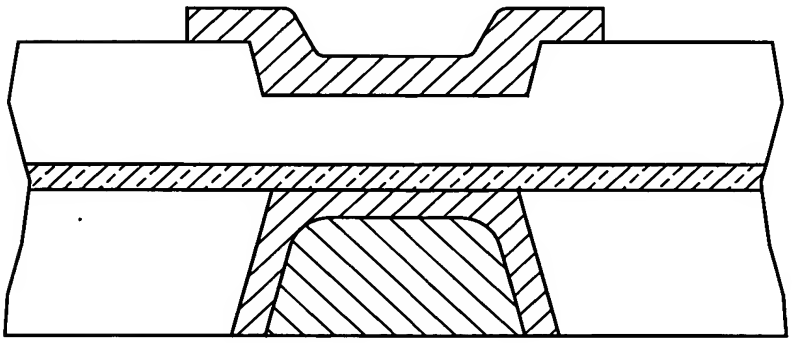

FIG. 3C

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE DARMAWAN

Application for Patent

Filed November 2, 2001

Serial No. 10/053,424

FOR:

SILICON ON INSULATOR DEVICE WITH IMPROVED HEAT REMOVAL (AS AMENDED)

APPEAL BRIEF

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on January 13, 2004 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signed: Kristina Gomez

BEYER WEAVER & THOMAS, LLP
Attorneys for Applicant

TABLE OF CONTENTS

Page No.

This is an appeal from the Office Action mailed October 27, 2003, finally rejecting claims 15 and 21-23 in the above-identified patent application. A copy of the claims on appeal are in the attached appendix.

I. REAL PARTY IN INTEREST

The real party in interest is Cree Microwave, Inc., by change of name from Ultra RF, Inc., of Sunnyvale, CA, assigned from Johan August Darmawan, inventor and applicant.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences

III. STATUS OF THE CLAIMS

Method claims 1-14 are being prosecuted in divisional patent application serial no. 10/327,479, device claims 16-20 are cancelled and claims 15 and 21-23 as amended remain in the application.

IV. STATUS OF AMENDMENTS

No amendment has been filed subsequent to this second final rejection.

V. SUMMARY OF INVENTION

The invention relates generally to silicon on insulator (SOI) semiconductor devices and manufacturing processing. As described in the background of the invention, reduced parasitic components can be achieved in semiconductor devices by fabrication of the devices in a silicon on insulator structure, such as silicon on sapphire and silicon on oxide insulator , including commercially available bonded silicon on insulator and implanted oxide (SIMOS). In such structures the supporting substrate is typically bonded to a heat sink for heat removal, which is particularly important for power transistor structures. Additionally, a ground plane can be provided by metallization on the substrate surface.

The claimed invention is directed to an SOI device having improved heat removal and with a structure which facilitates manufacture. With reference to Fig. 1D (copy as

exhibit 2 in the appendix) in one embodiment a component such as a transistor 16 is fabricated in silicon layer 14 which is supported by substrate 10 with a silicon oxide layer 12 therebetween. A heat sink for component 15 comprises a metal layer including refractory metal 20 and a metal layer 22. Metal layer 22 can be gold, copper, or aluminum, for example, which is compatible in semiconductor device and integrated circuit structures and manufacturing processes. The refractory metal 20 is optional in the structures.

An important feature of the invention is the provision of metal 20, 22 in a recessed portion of substrate 10 in close proximity to component 16 and insulated therefrom by silicon oxide layer 12. Further, as shown in Fig. 1c, the recessed portion in substrate 10 is formed by a preferential etchant which etches substrate 10 and with silicon oxide layer 12 functioning as an etchant stop, thereby preventing over etching into silicon oxide layer 12 and silicon layer 14.

Thus, in accordance with the invention as defined by claim 15, a metal layer is formed in the portion of the substrate in which silicon has been removed by etching, the metal layer abutting the silicon oxide layer and providing heat removal from the component, the silicon oxide layer electrically insulating the metal layer from the semiconductor component. Claims 21-23 further define the metal layer.

VI. ISSUES

Claim 15 has been finally rejected under 35 USC 102(e) as fully met and anticipated by Udrea et al., U.S. Patent Application Publication No. US 2002-0041003, the Examiner referring to Figs. 10a and 13c and the electrically insulating heat sink 45 in both figures.

Claims 21-23 have been finally rejected under 35 USC 103(a) as being unpatentable over Udrea et al. in view of Lin, U.S. Patent No. 6,483,147, the Examiner referring to Figs. 10a and 13c and paragraph **[0040]** of Udrea et al. and metal layer 52 in Lin.

The two issues in this appeal are whether Udrea et al. disclose the invention as defined by independent claim 15 and whether Udrea et al. can be modified by the teachings of Lin to suggest the invention as defined by dependent claims 21-23.

VII. GROUPING OF CLAIMS

The claims in each group stand together.

VIII. ARGUMENT

THE SILICON ON INSULATOR (SOI) SEMICONDUCTOR DEVICE AS DEFINED BY CLAIM 15 IS NOT DISCLOSED OR SUGGESTED BY UDREA ET AL.

The basic distinction between the device as defined by claim 15 and the device defined by Udrea et al. as shown in Figs. 10a and 13c is straight forward.

Claim 15 recites:

> a) a semiconductor body including a silicon supporting substrate, a silicon oxide layer supported by the substrate, and a silicon layer overlying the silicon oxide layer,
>
> b) a semiconductor component formed in the silicon layer overlying a portion of the substrate in which silicon has been removed by etching, and
>
> c) a **metal layer** in the portion of the substrate in which silicon has been removed by etching, the metal layer abutting the silicon oxide layer and providing heat removal from the component, **the silicon oxide layer electrically insulating the metal layer from the semiconductor component.** (Emphasis added).

The recited metal layer for heat removal is compatible with semiconductor device fabrication and facilitates heat removal by being placed close to the semiconductor component but electrically insulated therefrom.

Udrea et al. discloses in Figs. 10a and 13a an active structure 18 of a power device 10 which also includes an insulating membrane 16, also labeled 50 in Figs. 10a and 13c, and a heat sink material 45 contacting membrane 50. However, Udrea et al. expressly describes the heat sink material 45 as an insulating layer. See paragraphs **[0076]** and **[0079]**. Indeed, Udrea et al. describe heat layer 45 as diamond, aluminum oxide, boron nitride, or other materials with good electrically insulating properties and high thermal conductivity. See paragraphs **[0039]**, **[0074]** and **[0118]**, which are cited by the Examiner. Such insulating materials are not a metal layer as recited in claim 15 and are apparently intended to be transparent to infrared wavelengths, as suggested in paragraph **[0017]**. Accordingly, it is respectfully submitted that Udrea et al. do not show or suggest the semiconductor device as defined by claim 15.

DEPENDENT CLAIMS 21-23 ARE NOT SUGGESTED BY UDREA ET AL. IN VIEW OF LIN

Claims 21-23 depend from claim 15 and further define the metal layer of claim 15 as comprising a refractory metal, such as titanium tungsten and further comprising gold, aluminum or copper over the refractory metal.

Lin describes a backside metal contact to a SOI semiconductor device in which the contact comprises a conductive plug 38 that electrically contacts the semiconductor device 32 through a hole in silicon substrate layer 12 and insulation layer 34. Thus the contact is intended to be an electrical terminal of the device and necessarily physically and electrically contacts the device.

This is not the structure or function of the metal layer in the claimed invention where a silicon oxide layer electrically insulates the metal layer from the semiconductor component. While the invention leaves the insulating layer intact and thereby functions as an etch stop in etching the substrate, Lin intentionally removes the insulation layer so that the conductive plug 38 electrically and physically contacts the semiconductor device 32. This feature is specifically claimed by Lin, in particular reciting, "a conductive plug through the silicon substrate layer and the insulation layer contacting the silicon device layer, wherein the conductive plug extends into the silicon device layer."

Udrea et al. do suggest that the heat sink could be a bottom terminal of the semiconductor device and would be electrically and thermally conductive. This is similar to the conductive plug 38 of Lin which functions as a bottom terminal of the semiconductor device. However, in the claimed invention, the metal layer functions only as a heat sink and is expressly electrically insulated from the semiconductor component.

Accordingly, it is respectfully submitted that the teachings of Lin cannot be combined with Udrea et al. to suggest the invention as defined by claims 21-23.

IX. CONCLUSION

The silicon on insulator semiconductor device as defined by claims 15 and 21-23 is neither shown nor suggested by Udrea et al. alone or taken with Lin. The rejections of claims 15 and claims 21-23 under 35 USC 102(e) on Udrea et al., and under 35 USC 103(a) on Udrea et al. in view of Lin, should be reversed.

Respectfully Submitted,
BEYER WEAVER & THOMAS, LLP

Henry K. Woodward
Registration No. 22,672

BEYER WEAVER & THOMAS, LLP
P.O. Box 778
Berkeley, CA 94704-0778
(650) 961-8300

X. APPENDIX

CLAIMS ON APPEAL

Claims 1-14 (Withdrawn).

15. A silicon on insulator (SOI) semiconductor device comprising:

a) a semiconductor body including a silicon supporting substrate, a silicon oxide layer supported by the substrate, and a silicon layer overlying the silicon oxide layer,

b) a semiconductor component formed in the silicon layer overlying a portion of the substrate in which silicon has been removed by etching, and

c) a metal layer in the portion of the substrate in which silicon has been removed by etching, the metal layer abutting the silicon oxide layer and providing heat removal from the component, the silicon oxide layer electrically insulating the metal layer from the semiconductor component.

Claims 16-20 (Cancelled).

21. The semiconductor device and defined by claim 15, wherein the metal layer comprises a refractory metal.

22. The semiconductor device as defined by claim 21, wherein the metal layer comprises gold, aluminum, or copper over the refractory metal.

23. The semiconductor device as defined by claim 21, wherein the refractory metal comprises titanium tungsten.

FORMAL DRAWINGS

Formal Drawings are attached hereto.

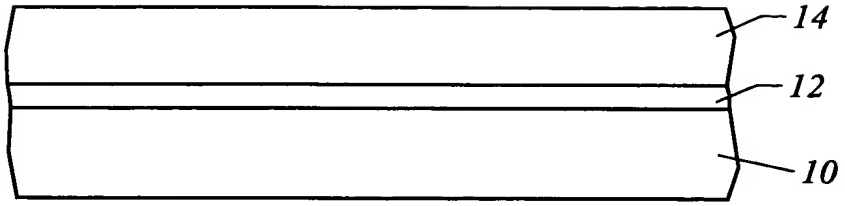

FIG. 1A

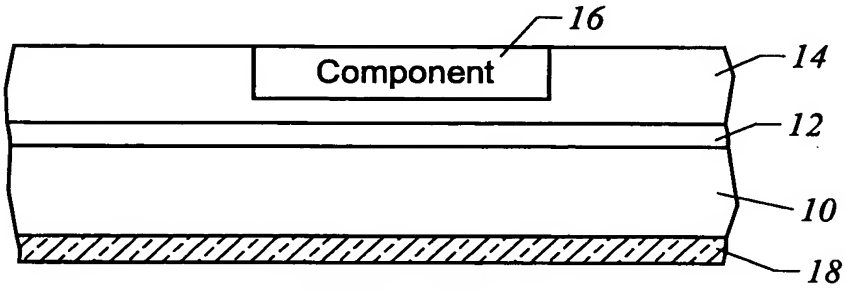

FIG. 1B

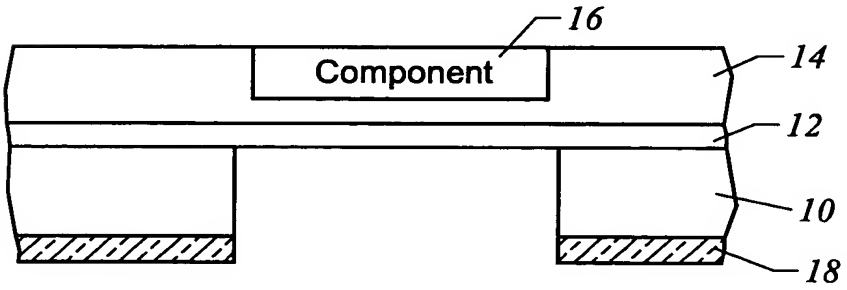

FIG. 1C

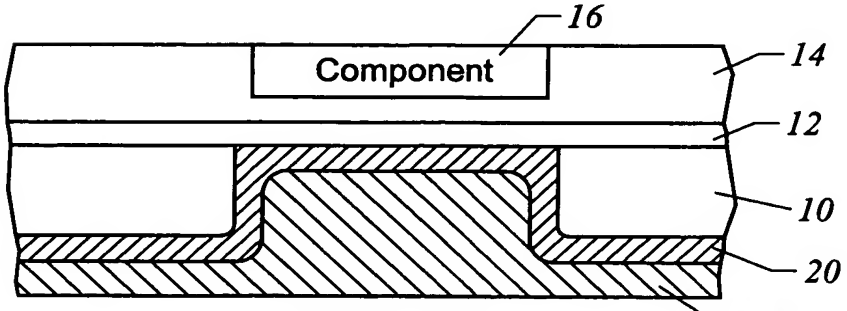

FIG. 1D

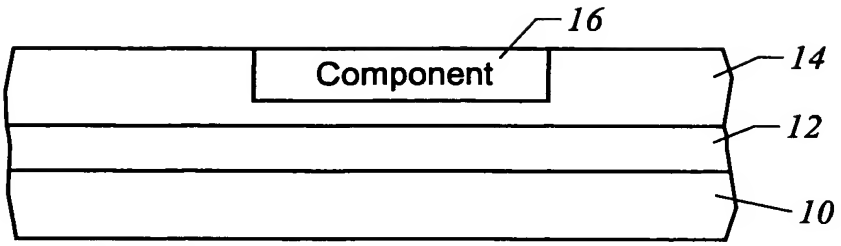

FIG. 2A

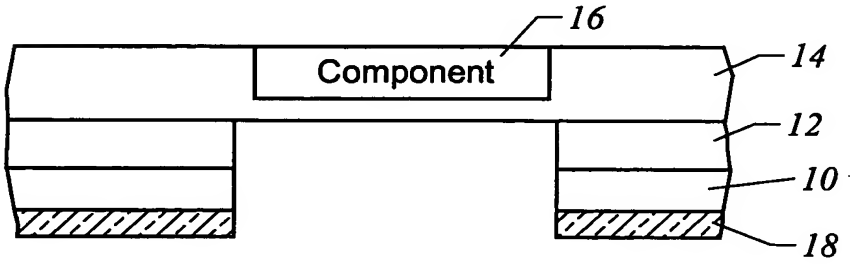

FIG. 2B

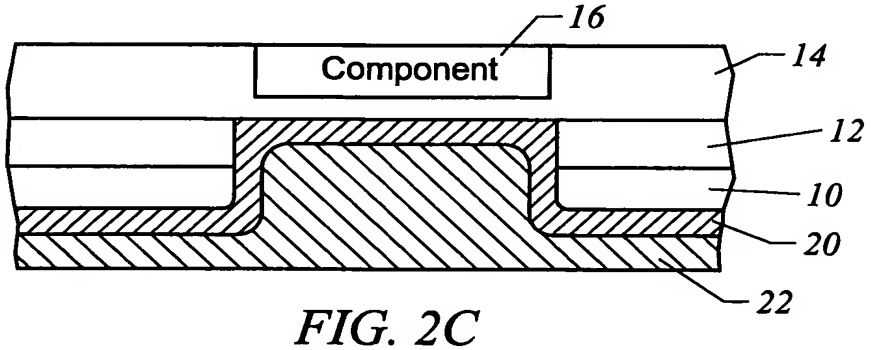

FIG. 2C

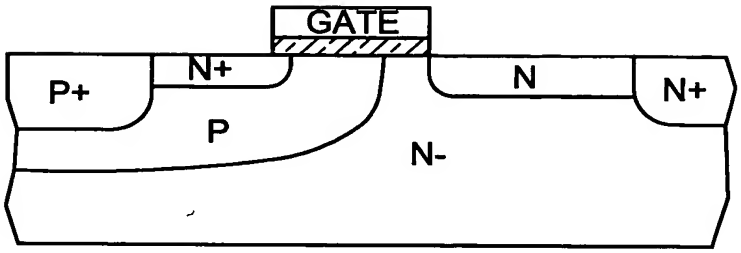

FIG. 3A

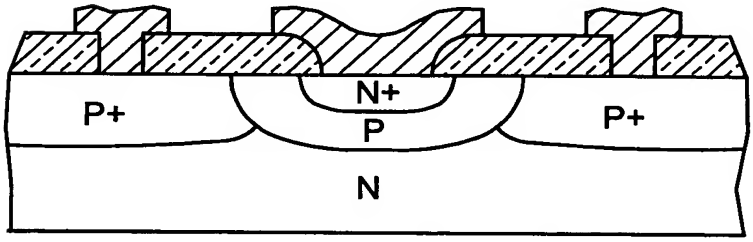

FIG. 3B

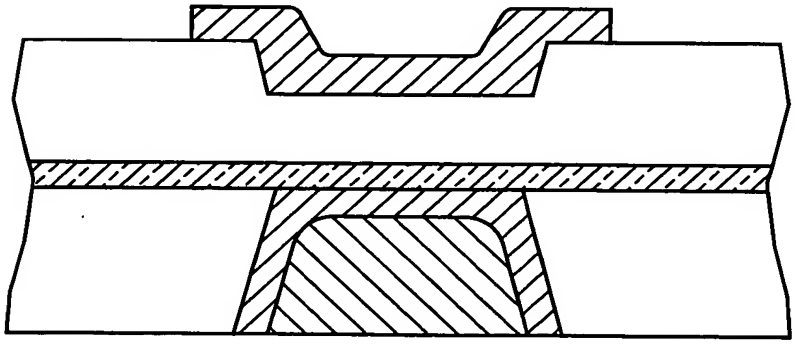

FIG. 3C